## Description

The XU devices are low phase noise quartz-based PLL oscillators supporting a large range of frequencies and output interface types. These devices are designed to operate at three different power supplies and are available in multiple package sizes as well as temperature grades.

With a patented one-time program (OTP) allowing for infinite memory shelf life, the XU devices can be programmed to generate an output frequency from 16kHz to 1500MHz with a resolution as low as 1Hz accuracy. The configuration capability of this family of devices allows for fast delivery times for both sample and large production orders.

## Pin Assignments

**NOTE**: To minimize power supply line noise, a 0.01µF bypass capacitor should be placed between $V_{DD}$ (Pin 6) and GND (Pin 3).

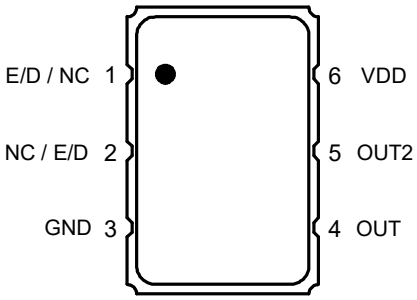



**Table 1. Pin Description**

| Pin # | Name | Description |
|---|---|---|
| 1 | E/D<br>NC | Enable/Disable [a][b]<br>No connect |
| 2 | NC<br>E/D | No connect<br>Enable/Disable [a][b] |
| 3 | GND | Connect to ground |
| 4 | OUT | Output |
| 5 | OUT2 | Complementary output [c] |
| 6 | $V_{DD}$ | Supply voltage |

[a] Pulled high internally = output enabled.

[b] Low = output disabled.

[c] Do not connect for LVCMOS. For XLVCMOS both OUT and OUT2 are ON and in opposite phase.

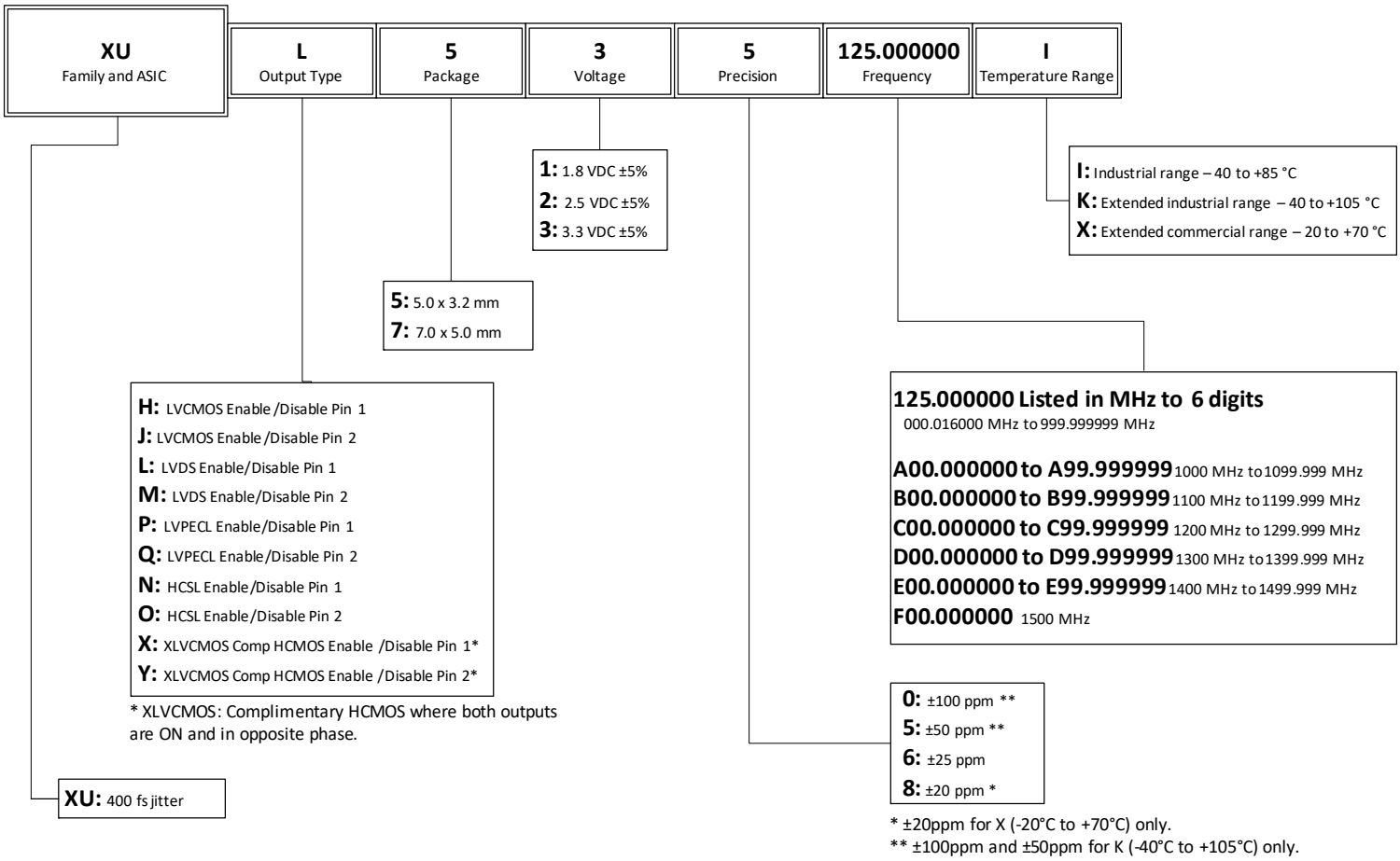
See Ordering Information for more details.

## Features

- Frequency range: 0.016MHz to 1500MHz[1]
- Output types: LVDS, LVPECL, HCSL, LVCMOS
- Supply voltage options: 1.8V, 2.5V, or 3.3V
- Phase jitter (1.875MHz to 20MHz): 100fs typical
- Phase jitter (12kHz to 20MHz): 300fs typical
- Package options:
  - 5.0 × 3.2 × 1.2 mm
  - 7.0 × 5.0 × 1.3 mm
- Operating temperature: -20°C to +70°C
  - Frequency stability options: ±20, ±25, ±50, or ±100 ppm
- Operating temperature: -40°C to +85°C
  - Frequency stability options: ±25, ±50, or ±100 ppm
- Operating temperature: -40°C to +105°C
  - Frequency stability options: ±50 or ±100 ppm

[1] There is a dead zone between 1037.5MHz to 1300MHz. Contact support for frequencies above 1300MHz.

# Ordering Information



# Contents

# Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the device. The ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

**Table 2. Absolute Maximum Ratings**

| Item | Rating | | | |
|---|---|---|---|---|
| $V_{DD}$ | -0.5 to +5.0V | | | |
| E/D | -0.5V to $V_{DD}$ + 0.5V | | | |
| OUT | -0.5V to $V_{DD}$ + 0.5V | | | |
| Storage Temperature | -55°C to 125°C | | | |
| Maximum Junction Temperature | 125°C | | | |
| Core Current | 65mA maximum | | | |
| Theta $J_A$ | JU6 | 75.9 °C/W | JS6 | 89.6 °C/W |
| Theta $J_B$ | | 48.6°C/W | | 54.3 °C/W |

# ESD Compliance

**Table 3. ESD Compliance**

| | |
|---|---|
| Human Body Model (HBM) | 1000V |

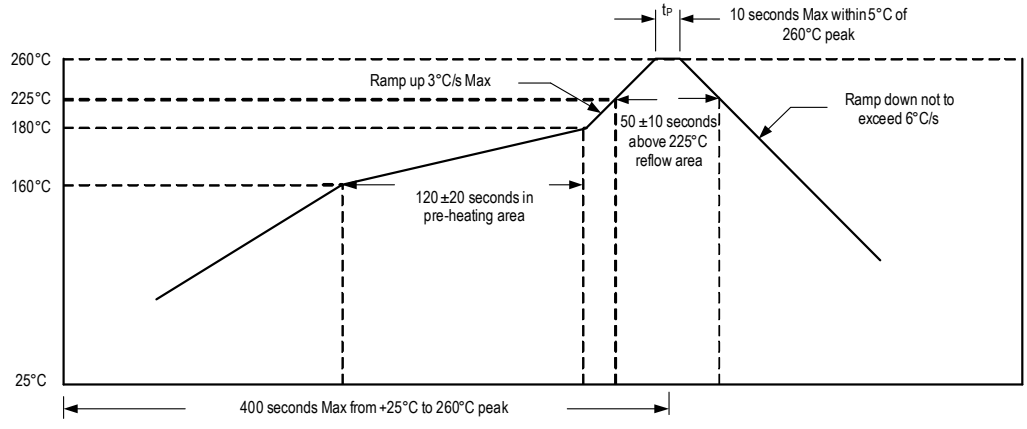
# Mechanical Testing

**Table 4. Mechanical Testing ***

| Parameter | Test Method |
|---|---|
| Mechanical Shock | Half-sine wave with 0.3ms 3000G. X, Y, Z each direction 1 time. |
| Mechanical Vibration | Frequency: 10 – 55MHz amplitude: 1.5mm.<br>Frequency: 55 – 2000Hz peak value: 20G.<br>Duration time: 4H for each X,Y,Z axis; total 12hours. |
| High Temp Operating Life (HTOL) | 2000 hours at 125°C (under power). |
| Hermetic Seal | Gross leak (air leak test). Fine leak (Helium leak test) He-pressure: 6kgf/cm² 2 hours. |

* MSL level does not apply.

# Solder Reflow Profile



# DC Electrical Characteristics

Note for all DC Electrical Characteristics tables: A pull-up resistor from $V_{DD}$ to E/D enables output when pin 1 is left open.

### Table 5. 3.3V IDD DC Electrical Characteristics

$V_{DD}$ = 3.3V ±5%, $T_A$ = -20°C to +70°C; -40°C to +85°C, -40°C to +105°C.

| Symbol | Parameter | Output Type | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ | Current Consumption | LVDS | 0.016MHz to 400MHz. | | | 97 | mA |
| | | | 400.000+MHz to 1.5GHz. | | | 122 | |
| | | LVPECL | 0.016MHz to 212.5MHz. | | | 115 | |
| | | | 212.5+MHz to 400MHz. | | | 128 | |
| | | | 400+MHz to 670MHz. | | | 142 | |
| | | HCSL | 0.016MHz to 670MHz. | | | 145 | |
| | | LVCMOS | 0.016MHz to 62.5MHz. | | | 98 | |
| | | | 62.5+MHz to 167MHz. | | | 108 | |

### Table 6. 2.5V IDD DC Electrical Characteristics

$V_{DD}$ = 2.5V ±5%, $T_A$ = -20°C to +70°C; -40°C to +85°C, -40°C to +105°C.

| Symbol | Parameter | Output Type | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ | Current Consumption | LVDS | 0.016MHz to 400MHz. | | | 90 | mA |
| | | | 400.000+MHz to 1.35GHz. | | | 103 | |
| | | LVPECL | 0.016MHz to 156.25MHz. | | | 102 | |
| | | | 156.25+MHz to 400MHz. | | | 112 | |
| | | | 400+MHz to 670MHz. | | | 118 | |
| | | HCSL | 0.016MHz to 400MHz. | | | 102 | |
| | | | 400.000+MHz to 670MHz. | | | 112 | |
| | | LVCMOS | 0.016MHz to 62.5MHz. | | | 80 | |
| | | | 62.5+MHz to 125MHz. | | | 85 | |
| | | | 125+MHz to 167MHz. | | | 92 | |

### Table 7. 1.8V IDD DC Electrical Characteristics

$V_{DD}$ = 3.3V ±5%, $T_A$ = -20°C to +70°C; -40°C to +85°C, -40°C to +105°C.

| Symbol | Parameter | Output Type | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ | Current Consumption | LVDS | 0.016MHz to 400MHz. | | | 65 | mA |
| | | | 400.000+MHz to 1.0GHz. | | | 72 | |
| | | LVPECL | 0.016MHz to 250MHz. | | | 75 | |
| | | | 250.000+MHz to 670MHz. | | | 97 | |
| | | HCSL | 0.016MHz to 400MHz. | | | 68 | |
| | | | 400.000+MHz to 670MHz. | | | 77 | |
| | | LVCMOS | 0.016MHz to 125MHz. | | | 58 | |

### Table 8. LVDS DC Electrical Characteristics

$V_{DD}$ = 3.3V, 2.5V, 1.8V ±5%, $T_A$ = -20°C to +70°C; -40°C to +85°C, -40°C to +105°C. Below are guaranteed for listed standard frequencies.

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OD}$ | Differential Output Voltage | | 0.25 | 0.4 | 0.5 | V |
| $V_{OS}$ | Output Offset Voltage | | 1 | 1.17 | 1.375 | |
| $V_{IH}$ | Enable/Disable Input High Voltage | | 70%$V_{DD}$ | | | |
| $V_{IL}$ | Enable/Disable Input Low Voltage | | | | 30%$V_{DD}$ | |

### Table 9. LVPECL DC Electrical Characteristics

$V_{DD}$ = 3.3V, 2.5V, 1.8V ±5%, $T_A$ = -20°C to +70°C; -40°C to +85°C, -40°C to +105°C. Below are guaranteed for listed standard frequencies.

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | $V_{DD}$ = 3.3V ±5%. | 1.85 | | 2.3 | V |
| | | $V_{DD}$ = 2.5V ±5%. | 1.1 | | 1.45 | |
| | | $V_{DD}$ = 1.8V ±5%. | 0.5 | | 0.8 | |
| $V_{OL}$ | Output Low Voltage | $V_{DD}$ = 3.3V ±5%. | 1.1 | | 1.65 | |
| | | $V_{DD}$ = 2.5V ±5%. | 0.35 | | 0.85 | |
| | | $V_{DD}$ = 1.8V ±5%. | 0 | | 0.25 | |
| $V_{IH}$ | Enable/Disable Input High Voltage | | 70%$V_{DD}$ | | | |
| $V_{IL}$ | Enable/Disable Input Low Voltage | | | | 30%$V_{DD}$ | |

### Table 10. HCSL DC Electrical Characteristics

$V_{DD}$ = 3.3V, 2.5V, 1.8V ±5%, $T_A$ = -20°C to +70°C; -40°C to +85°C, -40°C to +105°C. Below are guaranteed for listed standard frequencies.

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | $V_{DD}$ = 3.3V ±5%. | 0.6 | | 1.1 | V |
| | | $V_{DD}$ = 2.5V ±5%. | 0.55 | | 0.95 | |
| | | $V_{DD}$ = 1.8V ±5%. | 0.45 | | 0.7 | |
| $V_{OL}$ | Output Low Voltage | | 0 | | 0.2 | |
| $V_{IH}$ | Enable/Disable Input High Voltage | | 70%$V_{DD}$ | | | |
| $V_{IL}$ | Enable/Disable Input Low Voltage | | | | 30%$V_{DD}$ | |

### Table 11. LVCMOS DC Electrical Characteristics

$V_{DD}$ = 3.3V, 2.5V, 1.8V ±5%, $T_A$ = -20°C to +70°C; -40°C to +85°C, -40°C to +105°C. Below are guaranteed for listed standard frequencies.

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Differential Output Voltage | | 90%$V_{DD}$ | | | V |
| $V_{OL}$ | Output Offset Voltage | | | | 10%$V_{DD}$ | |
| $V_{IH}$ | Enable/Disable Input High Voltage | | 70%$V_{DD}$ | | | |
| $V_{IL}$ | Enable/Disable Input Low Voltage | | | | 30%$V_{DD}$ | |

# AC Electrical Characteristics

### Table 12. 3.3V AC Electrical Characteristics

$V_{DD}$ = 3.3V ±5%, $T_A$ = -20°C to +70°C; -40°C to +85°C, -40°C to +105°C.

| Symbol | Parameter | Test Condition | | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| F | Output Frequency Range | LVDS. | | 0.016 | | 1500 | MHz |
| | | LVPECL, HCSL. | | 0.016 | | 670 | |
| | | LVCMOS. | | 0.016 | | 167 | |
| | Frequency Stability | Temperature = -20°C to +70°C. | | ±20 | | ±100 | ppm |
| | | Temperature = -40°C to +85°C. | | ±25 | | ±100 | ppm |
| | | Temperature = -40°C to +105°C. | | ±50 | | ±100 | ppm |
| | Aging (1st year) | $T_A$ = 25°C. | | | | ±3 | |
| | Aging (10 years) | $T_A$ = 25°C. | | | | ±10 | |
| | Output Load | LVDS. | Differential. | | 100 | | Ω |
| | | LVPECL. | $V_{DD}$ - 2.0V. | | 50 | | |
| | | HCSL. | To GND. | | 50 | | |
| | | LVCMOS. | To GND. | | 15 | | pF |
| $T_{ST}$ | Start-up Time | Output valid time after $V_{DD}$ meets minimum specified level. | | | | 10 | ms |
| $t_R$ | Output Rise Time | LVDS. | 20% to 80% Vpk-pk. | | 275 | 380 | ps |
| | | LVPECL. | | | | 400 | |
| | | HCSL. | | | | 330 | |
| | | LVCMOS. | 10% to 90% $V_{DD.}$ | | | 3 | ns |
| $t_F$ | Output Fall Time | LVDS. | 80% to 20% Vpk-pk. | | 275 | 380 | ps |
| | | LVPECL. | | | | 400 | |
| | | HCSL. | | | | 330 | |
| | | LVCMOS. | 90% to 10% $V_{DD.}$ | | | 3 | ns |
| $O_{DC}$ | Output Clock Duty Cycle | LVDS. | | 45 | | 55 | % |
| | | LVPECL. | $F_{OUT} \leq$ 312.5MHz. | 45 | | 55 | |
| | | | $F_{OUT}$ > 312.5MHz. | 40 | | 60 | |
| | | HCSL. | | 45 | | 55 | |
| | | LVCMOS. | $F_{OUT} \leq$ 62.5MHz. | 45 | | 55 | |
| | | | $F_{OUT}$ > 62.5MHz. | 40 | | 60 | |
| $T_{OE}$ | Output Enable/ Disable Time | | | | | 100 | ns |
| $f_{JITTER}$ | Phase Jitter (12kHz–20MHz) | LVDS. | | | 300 | 400 | fsec |
| | | LVPECL. | | | 300 | 400 | |
| | | HCSL. | | | 300 | 400 | |
| | | LVCMOS. | $F_{OUT}$ = 100MHz. | | 300 | 400 | |

### Table 13. 2.5V AC Electrical Characteristics

$V_{DD}$ = 2.5V ±5%, $T_A$ = -20°C to +70°C; -40°C to +85°C, -40°C to +105°C.

| Symbol | Parameter | Test Condition | | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| F | Output Frequency Range | LVDS. | | 0.016 | | 1350 | MHz |
| | | LVPECL. | | 0.75 | | 670 | |
| | | HCSL. | | 0.016 | | 670 | |
| | | LVCMOS. | | 0.016 | | 167 | |
| | Frequency Stability | Temperature = -20°C to +70°C. | | ±20 | | ±100 | ppm |
| | | Temperature = -40°C to +85°C. | | ±25 | | ±100 | ppm |
| | | Temperature = -40°C to +105°C. | | ±50 | | ±100 | ppm |
| | Aging (1st year) | $T_A$ = 25°C. | | | | ±3 | |
| | Aging (10 years) | $T_A$ = 25°C. | | | | ±10 | |
| | Output Load | LVDS. | Differential. | | 100 | | Ω |
| | | LVPECL. | $V_{DD}$ - 2.0V. | | 50 | | |
| | | HCSL. | To GND. | | 50 | | |
| | | LVCMOS. | To GND. | | 15 | | pF |
| $T_{ST}$ | Start-up Time | Output valid time after $V_{DD}$ meets minimum specified level. | | | | 10 | ms |
| $t_R$ | Output Rise Time | LVDS. | 20% to 80% Vpk-pk. | | 300 | 400 | ps |
| | | LVPECL. | | | 250 | 630 | |
| | | HCSL. | | | | 315 | |
| | | LVCMOS. | 10% to 90% $V_{DD.}$ | | | 3 | ns |
| $t_F$ | Output Fall Time | LVDS. | 80% to 20% Vpk-pk. | | 300 | 400 | ps |
| | | LVPECL. | | | 360 | 630 | |
| | | HCSL. | | | | 315 | |
| | | LVCMOS. | 90% to 10% $V_{DD.}$ | | | 3 | ns |
| $O_{DC}$ | Output Clock Duty Cycle | LVDS. | | 45 | | 55 | % |
| | | LVPECL. | $F_{OUT} \leq$ 156.25MHz. | 45 | | 55 | |
| | | | $F_{OUT} \leq$ 156.25MHz. | 40 | | 60 | |
| | | HCSL. | | 45 | | 55 | |
| | | LVCMOS. | $F_{OUT} \leq$ 62.5MHz. | 45 | | 55 | |
| | | | $F_{OUT}$ > 62.5MHz. | 40 | | 60 | |
| $T_{OE}$ | Output Enable/ Disable Time | | | | | 100 | ns |
| $f_{JITTER}$ | Phase Jitter (12kHz–20MHz) | LVDS. | | | 400 | 500 | fsec |
| | | LVPECL. | | | 350 | 500 | |
| | | HCSL. | | | 350 | 500 | |
| | | LVCMOS. | $F_{OUT}$ = 100MHz. | | 350 | 500 | |

### Table 14. 1.8V AC Electrical Characteristics

$V_{DD}$ = 1.8V ±5%, $T_A$ = -20°C to +70°C; -40°C to +85°C, -40°C to +105°C.

| Symbol | Parameter | Test Condition | | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| F | Output Frequency Range | LVDS. | | 0.016 | | 1000 | MHz |
| | | LVPECL, HCSL. | | 0.016 | | 670 | |
| | | LVCMOS. | | 0.016 | | 125 | |
| | Frequency Stability | Temperature = -20°C to +70°C. | | ±20 | | ±100 | ppm |
| | | Temperature = -40°C to +85°C. | | ±25 | | ±100 | ppm |
| | | Temperature = -40°C to +105°C. | | ±50 | | ±100 | ppm |
| | Aging (1st year) | $T_A$ = 25°C. | | | | ±3 | |
| | Aging (10 years) | $T_A$ = 25°C. | | | | ±10 | |
| | Output Load | LVDS. | Differential. | | 100 | | Ω |
| | | LVPECL, HCSL. | To GND. | | 50 | | |
| | | LVCMOS. | To GND. | | 10 | | pF |
| $T_{ST}$ | Start-up Time | Output valid time after $V_{DD}$ meets minimum specified level. | | | | 10 | ms |
| $t_R$ | Output Rise Time | LVDS. | 20% to 80% Vpk-pk. | | 250 | 315 | ps |
| | | LVPECL. | | | 250 | 350 | |
| | | HCSL. | | | | 320 | |
| | | LVCMOS. | 10% to 90% $V_{DD.}$ | | 5 | | ns |
| $t_F$ | Output Fall Time | LVDS. | 80% to 20% Vpk-pk. | | 250 | 315 | ps |
| | | LVPECL. | | | 250 | 350 | |
| | | HCSL. | | | | 320 | |
| | | LVCMOS. | 90% to 10% $V_{DD.}$ | | 5 | | ns |
| $O_{DC}$ | Output Clock Duty Cycle | LVDS. | $F_{OUT} \leq$ 156.25MHz. | 45 | | 55 | % |
| | | | $F_{OUT} \leq$ 156.25MHz. | 40 | | 60 | |
| | | LVPECL. | $F_{OUT} \leq$ 312.5MHz. | 45 | | 55 | |
| | | | $F_{OUT}$ > 312.5MHz. | 40 | | 60 | |
| | | HCSL. | | 40 | | 60 | |
| | | LVCMOS. | $F_{OUT} \leq$ 62.5MHz. | 45 | | 55 | |
| | | | $F_{OUT}$ > 62.5MHz. | 40 | | 60 | |
| $T_{OE}$ | Output Enable/ Disable Time | | | | | 100 | ns |
| $f_{JITTER}$ | Phase Jitter (12kHz–20MHz) | LVDS. | | | 800 | 1200 | fsec |
| | | LVPECL. | | | 750 | 1200 | |
| | | HCSL. | | | 100 | 1200 | |
| | | LVCMOS. | $F_{OUT}$ = 100MHz. | | 800 | 1200 | |

**Notes for all AC Electrical Characteristics tables:**

[1] A pull-up resistor from $V_{DD}$ to E/D enables output when pin 1 is left open.

[2] Installation should include a 0.01µF bypass capacitor placed between VDD and GND to minimize power supply line noise.

[3] Stability is inclusive of 25°C tolerance, operating temperature range, input voltage change, load change, aging, shock and vibration.

[4] Standard LVCMOS frequencies include 10MHz, 12MHz, 12.288MHz, 16MHz, 20MHz, 24MHz, 24.576MHz, 25MHz, 33.333MHz, 40MHz, 48MHz, 50MHz, 100MHz, 125MHz and 156.25MHz.

[5] Standard differential frequencies include 100MHz, 106.25MHz, 125MHz, 150MHz, 155.52MHz, 156.25MHz, 200MHz, 212.5MHz, 250MHz, 300MHz, 312.5MHz and 400MHz.

# I2C Bus Characteristics

### Table 15. I2C Bus DC Characteristics

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Level | — | 0.7 × $V_{DD33}$ | — | — | V |
| $V_{IL}$ | Input Low Level | — | — | — | 0.3 × $V_{DD33}$ | V |

### Table 16. I2C Bus AC Characteristics

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $F_{SCLK}$ | Serial Clock Frequency (SCL) | — | — | 100 | 400 | kHz |
| $t_{BUF}$ | Bus Free Time between STOP and START | — | 1.3 | — | — | µs |
| $t_{SU:START}$ | Setup Time, START | — | 0.6 | — | — | µs |
| $t_{HD:START}$ | Hold Time, START | — | 0.6 | — | — | µs |
| $t_{SU:DATA}$ | Setup Time, Data Input (SDA) | — | 100 | — | — | µs |
| $t_{HD:DATA}$ | Hold Time, Data Input (SDA) [1] | — | 0 | — | — | µs |
| $t_R$ | Rise Time, Data and Clock (SDA, SCL) | — | — | — | 300 | ns |
| $t_F$ | Fall Time, Data and Clock (SDA, SCL) | — | — | — | 300 | ns |
| $t_{HIGH}$ | High Time, Clock (SCL) | — | 0.6 | — | — | µs |
| $t_{LOW}$ | Low Time, Clock (SCL) | — | 1.3 | — | — | µs |
| $t_{SU:STOP}$ | Setup Time, STOP | — | 0.6 | — | — | µs |

[1] A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

# Output Waveforms

**Figure 1. LVDS Output Waveforms**

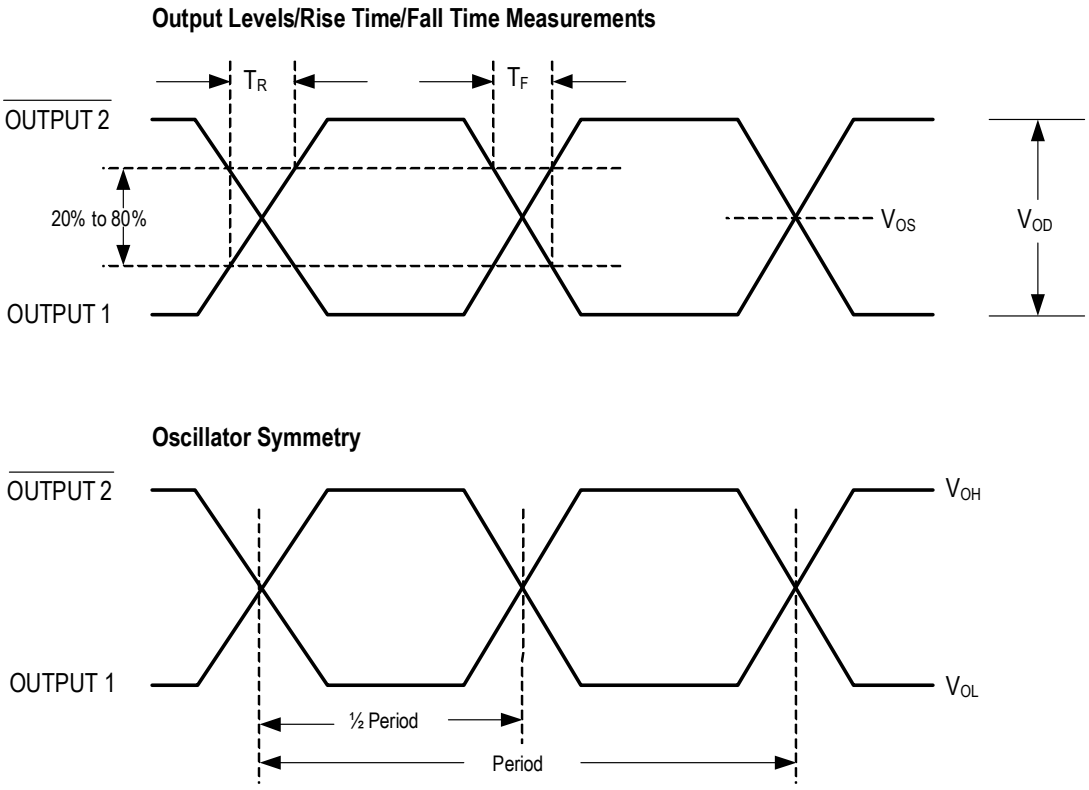



**Figure 2. LVPECL Output Waveforms**

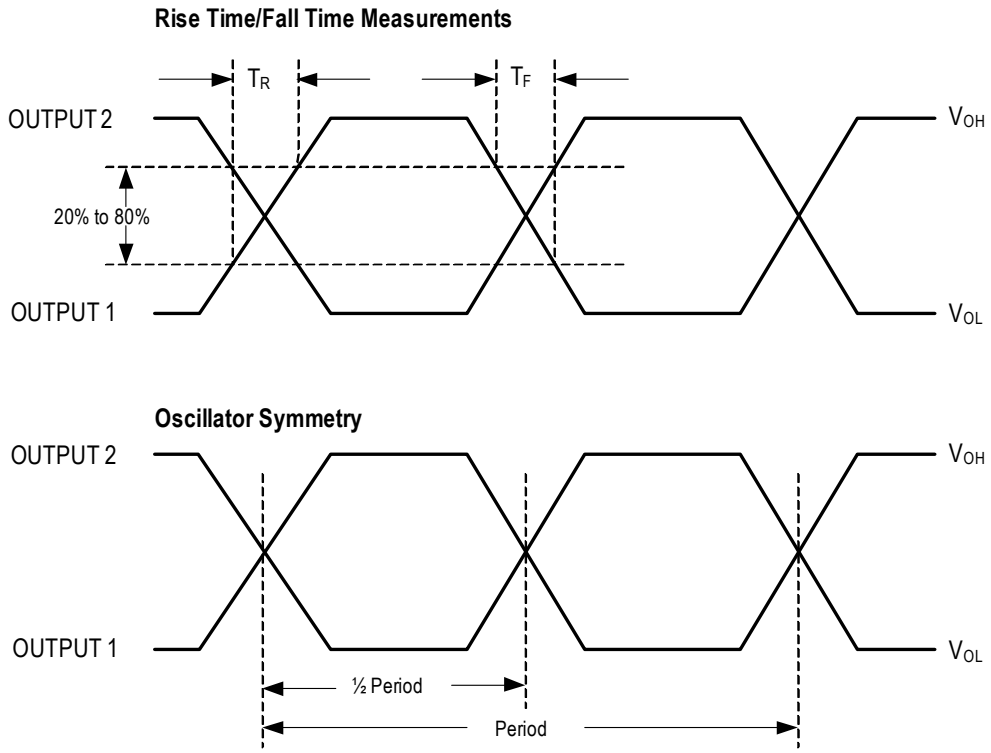


**Figure 3. HCSL Output Waveforms**

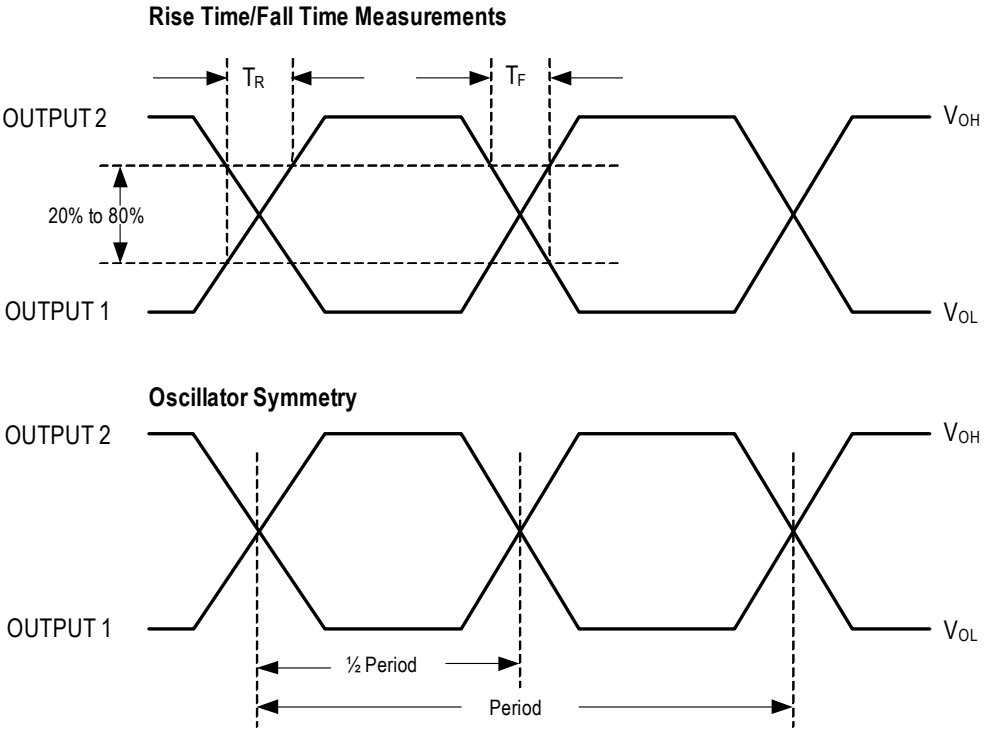
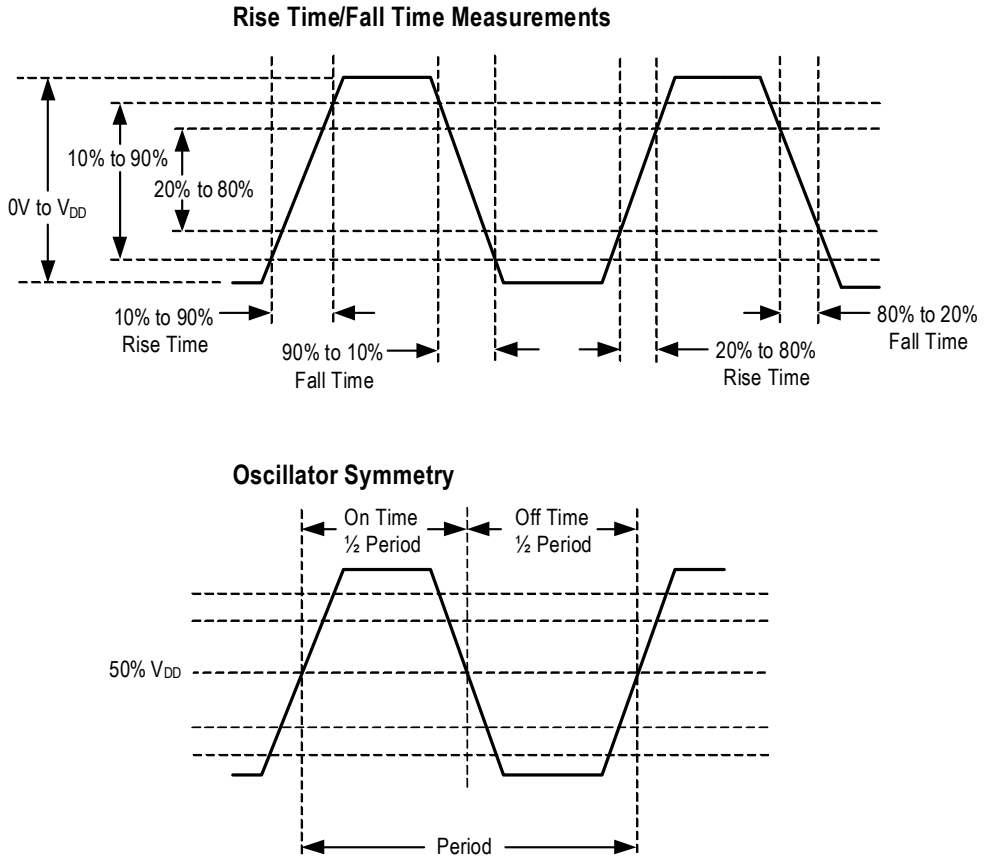



**Figure 4. LVCMOS Output Waveforms**

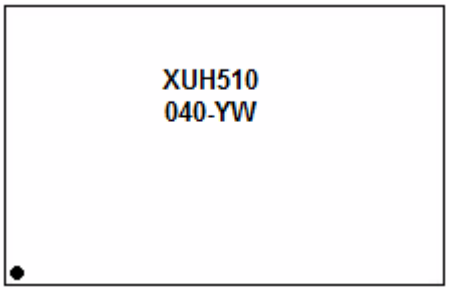


# Package Outline Drawings

The package outline drawings (JS6, JU6) are appended at the end of this document. The package information is the most current data available.

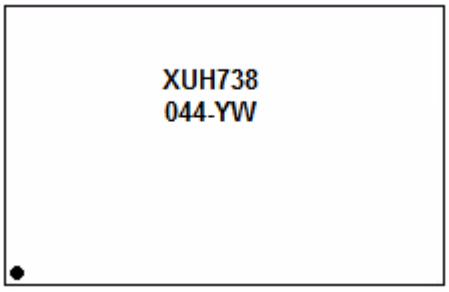
# Marking Diagrams

**JS6 5.0 × 3.2 mm Package Option** (example based on XUH510040.000000I)




- Line 1:
  - "XU" = family; "H" = output type; "5" = package size; "1" = voltage; "0" = precision level. This number will vary depending upon the output type, voltage, and precision values selected in the orderable part number.
- Line 2:
  - "040" denotes last three digits to the left of the decimal point as shown in the above example. This number will vary depending upon the frequency value selected in the orderable part number.
  - "YW" denotes the last digit of the year and work week the part was assembled.

**JU6 7.0 × 5.0 mm Package Option** (example based on XUH738044.736000X)

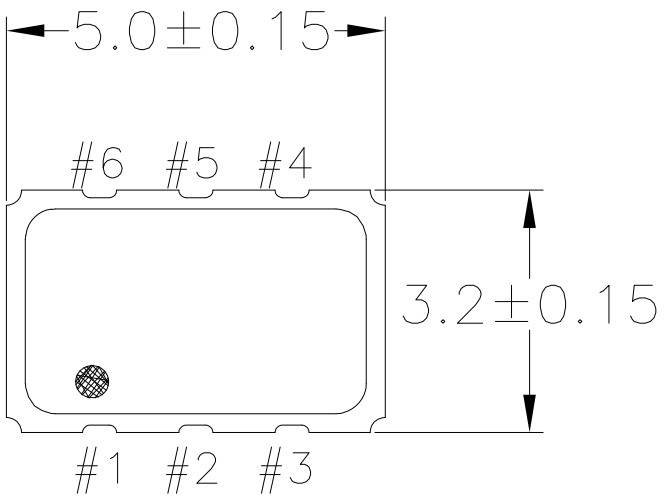



- Line 1:
  - "XU" = family; "H" = output type; "7" = package size; "3" = voltage; "8" = precision level. This number will vary depending upon the output type, voltage, and precision values selected in the orderable part number.
- Line 2:
  - "044" denotes last three digits to the left of the decimal point as shown in the above example. This number will vary depending upon the frequency value selected in the orderable part number.
  - "YW" denotes the last digit of the year and work week the part was assembled.

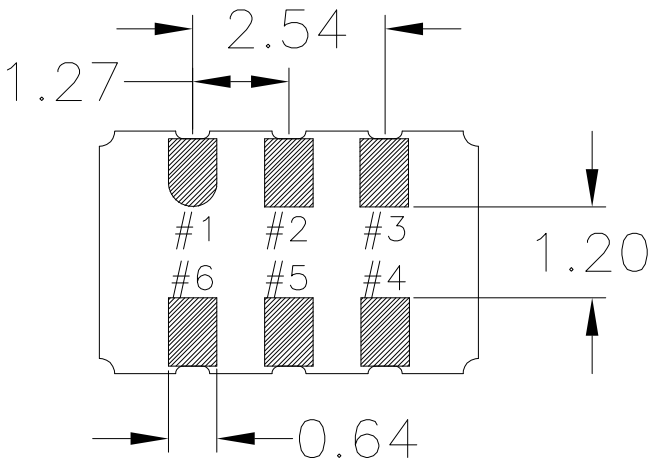
# Revision History

| Revision Date | Description of Change |
|---|---|
| August 18, 2021 | Moved Ordering Information table to just after Pin Descriptions. |
| January 19, 2021 | ▪ Removed 4-pin package description table, figure, and package drawing references.<br>▪ Added footnote for pin 5 in Table 1.<br>▪ Added footnote under “Output Type” in Ordering Information. |
| January 12, 2021 | Added Marking Diagrams section and updated Package Outline Drawings links. |
| February 11, 2020 | Added I2C Bus Characteristics tables. |
| June 28, 2019 | ▪ Added footnote to frequency range bullet under front page Features. |
| June 25, 2018 | ▪ Updated Package Outline Drawings section. |
| November 22, 2017 | ▪ Updated Theta JA and JB in Absolute Maximum Ratings table.<br>▪ Added MSL statement under Mechanical Testing table.<br>▪ Updated ordering information. |
| October 19, 2017 | ▪ Updated document title.<br>▪ Updated Features bullets.<br>▪ Updated Absolute Maximum Ratings and ESD Compliance tables.<br>▪ Added -40°C to +105°C rating to all electrical tables.<br>▪ Removed phase noise charts.<br>▪ Updated Ordering Information table. |
| May 12, 2017 | ▪ Reformatted embedded tables.<br>▪ Removed “Jitter Performance” tables and moved the “Phase Jitter (12kHz–20MHz)” parameter to its respective AC Electrical Characteristics table.<br>▪ Updated all Output Waveform drawings. |
| December 1, 2016 | Initial release. |

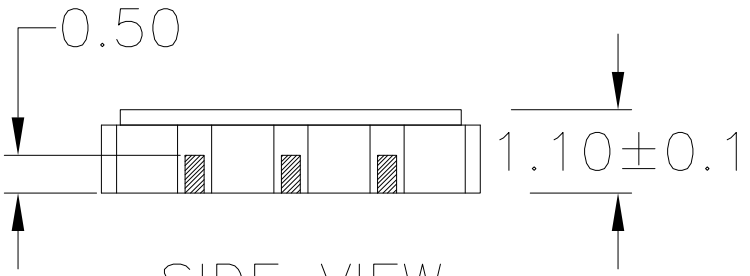
| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 04/2/12 | DP |
| 01 | ADDED LID IN TOP VIEW | 07/12/12 | KS |
| 02 | UPDATED LID TOLERANCES | 12/03/12 | KS |
| 03 | UPDATE PACKAGE DRAWING | 8/8/14 | J.HUA |




TOP VIEW




BOTTOM VIEW




SIDE VIEW

NOTES:

1. ALL DIMENSIONS IN MM.

| | | | |
|---|---|---|---|
| TOLERANCES UNLESS SPECIFIED<br>DECIMAL ANGULAR<br>XX± ±<br>XXX±<br>XXXX± | | IDT™ www.IDT.com | 6024 Silver Creek Valley Rd<br>San Jose, CA 95138<br>PHONE: (408) 727-6116<br>FAX: (408) 492-8674 |
| APPROVALS | DATE | TITLE | JS6 PACKAGE OUTLINE<br>5.0 x 3.2 mm BODY<br>1.1 mm Thick |
| DRAWN RAC | 04/2/12 | | |
| CHECKED | | | |
| | | SIZE C | DRAWING No. PSC-4411 REV 03 |
| | | DO NOT SCALE DRAWING | SHEET 1 OF 2 |

| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 04/2/12 | DP |
| 01 | ADDED LID IN TOP VIEW | 07/12/12 | KS |
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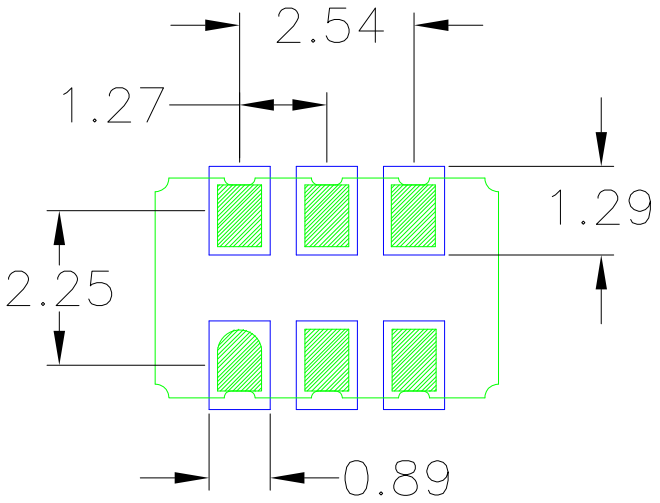


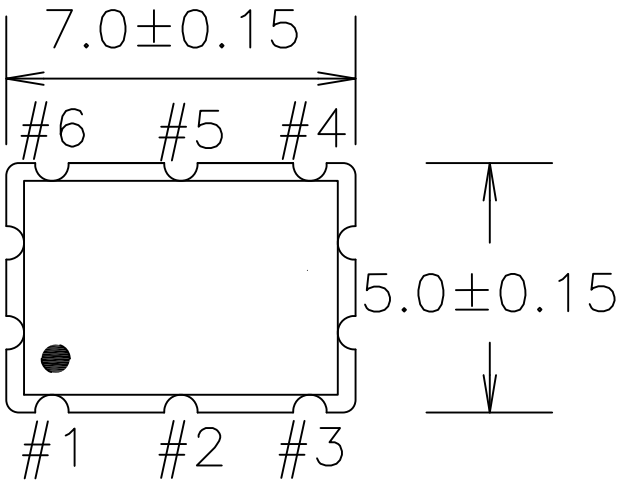

RECOMMENDED LAND PATTERN

NOTES:

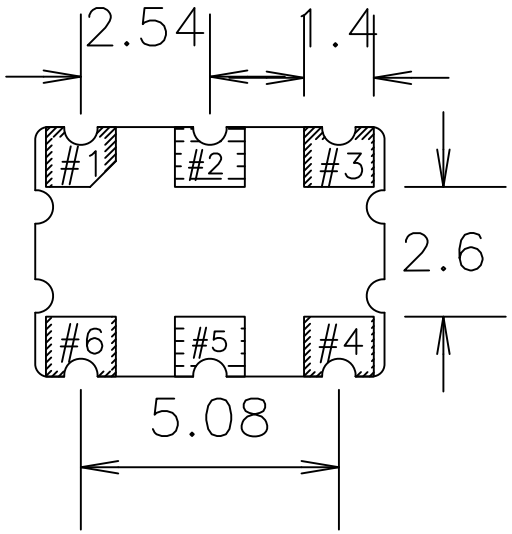
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| | | | |
|---|---|---|---|
| TOLERANCES UNLESS SPECIFIED<br>DECIMAL ANGULAR<br>XX± ±<br>XXX±<br>XXXX± | | IDT™ www.IDT.com | 6024 Silver Creek Valley Rd<br>San Jose, CA 95138<br>PHONE: (408) 727-6116<br>FAX: (408) 492-8674 |
| APPROVALS | DATE | TITLE | JS6 PACKAGE OUTLINE<br>5.0 x 3.2 mm BODY<br>1.1 mm Thick |
| DRAWN PEAC | 04/2/12 | | |
| CHECKED | | | |
| | | SIZE C | DRAWING No. PSC-4411 REV 03 |
| | | DO NOT SCALE DRAWING | SHEET 2 OF 2 |

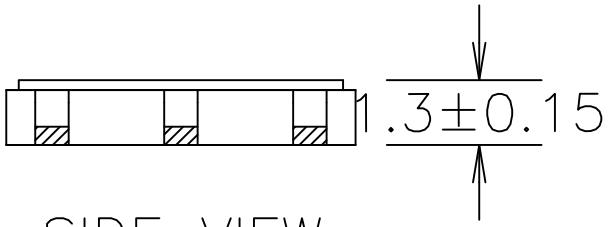
| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 10/5/12 | KS |
| 01 | UPDATE PACKAGE DRWING | 8/12/14 | J.HUA |




TOP VIEW




BOTTOM VIEW



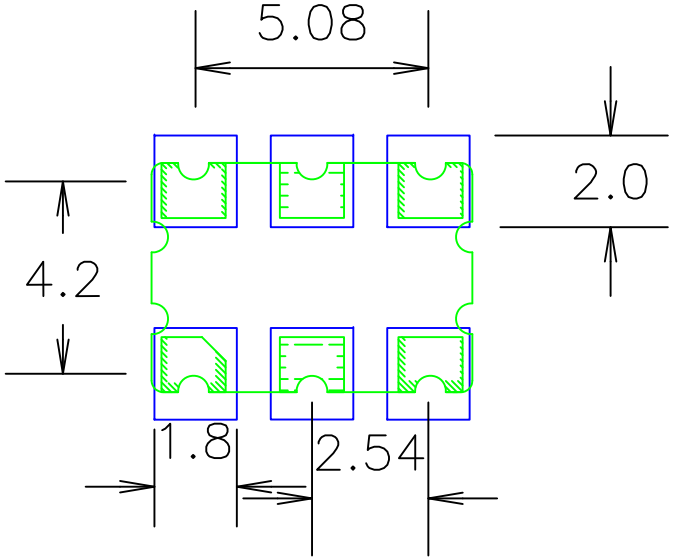

SIDE VIEW

NOTES:

1. ALL DIMENSIONS IN MM.

| | | | |
|---|---|---|---|
| TOLERANCES UNLESS SPECIFIED<br>DECIMAL ANGULAR<br>XX± ±<br>XXX±<br>XXXX± | | IDT™ www.IDT.com | 6024 Silver Creek Valley Rd<br>San Jose, CA 95138<br>PHONE: (408) 727-6116<br>FAX: (408) 492-8674 |
| APPROVALS | DATE | TITLE | JU6 PACKAGE OUTLINE<br>7.0 x 5.0 mm BODY<br>1.3 mm Thick |
| DRAWN KB | 10/03/12 | | |
| CHECKED | | SIZE C | DRAWING No. PSC-4430 REV 01 |
| | | DO NOT SCALE DRAWING | SHEET 1 OF 2 |

| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 10/5/12 | KS |
| 01 | UPDATE PACKAGE DRWING | 8/12/14 | J.HUA |




RECOMMENDED LAND PATTERN

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| | | | |
|---|---|---|---|
| TOLERANCES UNLESS SPECIFIED<br>DECIMAL ANGULAR<br>XX± ±<br>XXX±<br>XXXX± | | IDT™ www.IDT.com | 6024 Silver Creek Valley Rd<br>San Jose, CA 95138<br>PHONE: (408) 727-6116<br>FAX: (408) 492-8674 |
| APPROVALS | DATE | TITLE JU6 PACKAGE OUTLINE<br>7.0 x 5.0 mm BODY<br>1.3 mm Thick | |
| DRAWN JCB | 10/03/12 | | |
| CHECKED | | | |
| | | SIZE C / DRAWING No. PSC-4430 | REV 01 |
| | | DO NOT SCALE DRAWING | SHEET 2 OF 2 |

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(Rev.1.0 Mar 2020)


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